

B10

ABSTRACT

An asynchronous FIFO circuit has
a memory;

asynchronous reading and writing means of reading a
predetermined amount of data from and of reading the
predetermined amount of data into the memory on a
first-in-first-out basis;

an error write counter of counting counts up by 1 if the
predetermined amount of data written into the memory contains
an error;

an error read counter of counting up by 1 if the
predetermined amount of data read from the memory contains
an error;

comparing means of comparing a value of the error write
counter with a value of the error read counter, the comparing
means outputting a logic level of 0 when the value of the error
write counter is coincident with the value of the error read
counter, the comparing means outputting a logic level of 1
if the former value is different from the latter value.

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